ABSTRACT OF THE DISCLOSURE

A semiconductor device memory cell (**100**) can include a built-in capacitor for reducing a soft-error rate (SER). A memory cell (**100**) can include a first inverter (**102**) and second inverter (**104**) arranged in a cross-coupled configuration. A capacitor (**110**) can be coupled between a first storage node (**106**) and second storage node (**108**). A capacitor (**110**) can be a "built-in" capacitor formed with interconnect wirings utilized to connect memory cell circuit components.